## Remarks

Claims 1, 7, 12, and 17 have been amended, and new Claims 25-28 have been added. Therefore, Claims 2-5, 7-10, 12-15, 17-20 and 25-28 are currently pending in this application. The Examiner's reconsideration of all outstanding rejections is respectfully requested, particularly in view of the above amendments and the following remarks.

Claims 2-5, 7-10, 12-15 and 17-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,804,134 to Proebsting. Claims 1, 7, 12 and 17 have been amended. No new matter has been added.

Amended Claim 2 recites, *inter alia,* a "content addressable memory ("CAM") system comprising a plurality of segments arranged in an array . . . each matchline and sinkline being shared by all of the CAM cells in a same segment . . . wherein each matchline has substantially the same capacitance as each other matchline." Support for this amendment is inherent in the Application as originally filed. *See also,* Application at page 2, lines 14-15; page 3, lines 14-17; page 4, lines 10-12 and 15-17; page 8, lines 6-9 and 23-26; page 9, lines 20-24. No new matter has been added.

The '134 to Proebsting et al. is generally directed towards a content addressable memory ("CAM") having array blocks. Proebsting et al. fairly show that the CAM array may be reduced into successive blocks having increasing numbers of CAM cells, and that the resulting successive blocks of increasing length may have power savings advantages over non-blocked arrays.

The Examiner has suggested that the array blocks or segments of Proebsting may include equal numbers of CAM cells, while Applicants maintain that Proebsting only suggests that the *increase* in size for successive blocks might be an arbitrary positive (i.e., non-zero) integer. All of Proebsting's embodiments and claimed power-savings advantages are directed towards hierarchical segments of increasing size (e.g., +2, +6, etc.). Thus, a broad interpretation of Proebsting might fairly hold that the particular *increase* in size for successive segments might be an arbitrary positive, but non-zero, integer. *See* Proebsting at col. 4, lines 57-60; col. 5, lines 36-39.

Proebsting et al. utterly fail to recognize, much less address, the matchline capacitance issue. In addition, Proebsting et al. fail to recognize, address or motivate the processing speed advantages of equal capacitances, or the circuitry advantages such as simplified clock circuitry made possible when "each matchline has substantially the same capacitance as each other matchline", as recited in Applicants' amended Claim 2.

Embodiments disclosed by Applicants offer distinct advantages over the prior art. Applicants provide that each matchline has substantially the same capacitance, which may be achieved when each matchline connects to a constant number of CAM cells, for example. Thus, in Applicants' presently claimed subject matter, the maximum matchline capacitance stays the same as array sizes are increased. Both the non-segmented teachings of the prior art and the increasing array blocks of Proebsting et al. only show embodiments where matchline capacitance increases as the CAM array gets wider.

Thus, as the CAM widths or numbers of cells increase, Applicants' presently claimed embodiments substantially avoid the decreased operating speed and increased circuit complexity of conventional CAM architectures. This feature of substantially fixed matchline capacitance is patentably distinguishable over prior art such as Proebsting, in which some matchlines are connected to a greater number of CAM cells as the width of the CAM array is increased, thus slowing the processing speed of wider CAM arrays.

In addition, Applicants' presently claimed embodiments may have improved speed over those of Proebsting, particularly for partial matches. When the first segment matches, subsequent array blocks or segments in Proebsting may take a greater number of clock cycles per segment due to the increasing matchline capacitance, while each of Applicants' subsequent segments take about the same amount of time due to the substantially same matchline capacitances, for example. Thus, Applicants' clock frequency may be optimized to the constant time per segment.

Therefore, amended Claim 2 is neither taught nor suggested by the '134 to Proebsting et al. Similarly, amended Claims 7, 12 and 17, which each recite like features, are also neither taught nor suggested by the '134 to Proebsting et al., whether taken alone or in combination with any of the other references of record in this case.

New Claims 25-28 have been added. Support for new Claims 25-28 is present in the Application as originally filed. *See, e.g.,* Application at page 6, line 27 through page 7, line 10. No new matter has been added.

New Claim 25 recites, *inter alia,* "a flip-flop with output connected to the dedicated sinkline and inputs connected only to a previous segment sinkline, a previous segment matchline, and a same system clock for all segments, respectively."

The '134 to Proebsting et al. teaches non-equal array blocks or segments, where "L<M<N" (see, e.g., Proebsting at col. 4, lines 57-60; col. 5, lines 36-39). While Proebsting may address saving power by increasing array block widths, Applicants teach that the increased segment widths would have greater capacitance. Thus, Proebsting has the problem of increased matchline and/or sinkline times for successive array blocks. Proebsting fails to recognize or address the problem with increased capacitance for increased array block width.

The '134 to Proebsting et al. fails to show the associated clock circuitry, which would be required to address the increasing matchline and/or sinkline times for successive array blocks. It is respectfully submitted that the CAM array blocks of Proebsting would require rather complex clock circuitry to support Proebsting's array blocks of increasing width or cell count. In particular, unless processing speed was thrown to the wind by using a delayed system clock to match only the worst-case or widest block, the same system clock could not be used as the enabling input for more than one width of array block.

Therefore, new Claim 25 is neither taught nor suggested by the '134 to Proebsting et al. Similarly, new Claims 26-28, which each recite like features, are also neither taught nor suggested by the '134 to Proebsting et al., whether taken alone or in combination with any of the other references of record in this case.

Conclusion

Accordingly, it is respectfully submitted that amended independent Claims 2, 7, 12 and 17 are in condition for allowance for at least the reasons stated above. Since the remaining dependent claims each depend from one of the above claims and necessarily include each of the elements and limitations thereof, it is respectfully submitted that these claims are also in condition for allowance for at least the reasons stated, as well as for reciting additional patentable subject matter. Thus, each of Claims 2-5, 7-10, 12-15, 18-20 and 25-28 is in condition for allowance. All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case are earnestly solicited.

Respectfully submitted,

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